

MultiLynx™ CL2151 Universal HFC Interactive Cable Transceiver



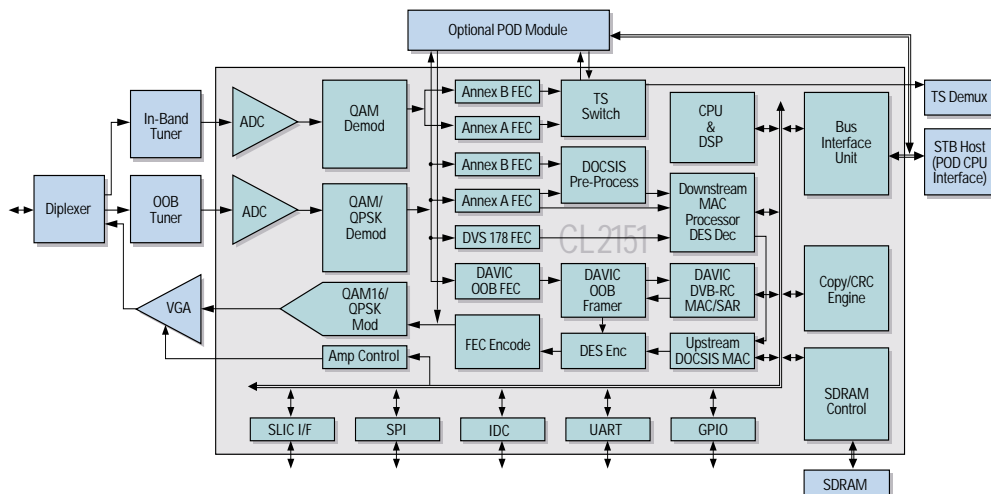
OVERVIEW

The MultiLynx™ CL2151 is a universal cable transceiver solution for advanced set-top boxes (STB) and cable modems compliant with DVB/DAVIC, and DOCSIS standards. The CL2151 is built for STB and cable-modem manufacturers requiring the maximum performance with the lowest system BOM cost. Its high level of integration provides manufacturers with a flexible, yet quick time-to-market solution for standards-based deployments all over the world.

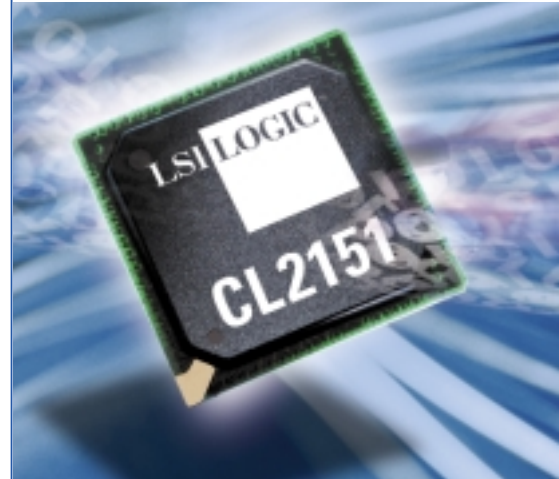
The CL2151 is a complete and highly integrated solution combining a 16-256 QAM in-band receiver, QPSK/QAM receiver for out-of-band downstream reception, a QPSK/16-QAM burst transmitter, and a proven DAVIC/DVB and DOCSIS 1.0/1.1 media access controller (MAC). The chip includes a RISC processor with a DSP instruction set enabling glueless interface to subscriber line ICs (SLICs) and a POD interface.

The CL2151 inband demodulator is a 16-256 QAM. A second out-of-band downstream channel provides an option to use a QPSK or full 16-256 QAM demodulation, allowing for flexible implementation for DOCSIS, DVB/DAVIC or DVS 178 without changing any external components. Both channels are compliant with ITU J.83 Annex A, B, and C and integrate a 10-bit A/D converter. The upstream QPSK/16-QAM burst transmitter along with ITU J.112 Annex A, B compliant FEC encoding provides a robust and cost-effective solution for DVB/DAVIC, and DOCSIS applications.

The hardware MAC (with packet parsing, filtering, and decryption), and the two internal processors – an 88 MHz mini-RISC and 117 MHz SPARC v8 processor, upon which the standard specific MAC software is executed – allow for flexible implementation of DVB In-Band, DOCSIS, or EuroDOCSIS standards.



High-Level Block Diagram of MultiLynx™ CL2151



INTERFACE FEATURES:

- OpenCable™ compliant by supporting OOB data to be bypassed to a POD interface for MAC processing
- PHY DES implementation for physical security compliant to the OpenCable and DVB standards
- Powerful SPARC v8 internal processor offloads the STB host processor from the MAC software tasks and provides a DSP capability for IP telephony applications
- Internal processor includes a DSP instruction set necessary for IP telephony applications
- Delivers a video telephony solution simply by adding uLAW or aLAW audio codec, aSLIC chipset and an MPEG video source encoder/decoder

Multilynx™ CL2151 Universal HFC Interactive Cable Transceiver

In Band Receiver	
Standards Compliance	DVB-C, ITU-T J.83 Annexes A, B, and C
A/D Converter	Internal 10-bit
Symbol Rate	Variable from 1 – 7.2 Mbaud
QAM Constellations	16, 32, 64, 128, 256 QAM (including DAVIC 256 QAM Map)
IF Input Frequencies	36 MHz or 44 MHz IF inputs
Output	Multiplexed transport stream output with forward channel
Additional I/O	Point of Deployment (POD) MPEG out to POD, in from POD, and out to Demux*
Forward Interactive Channel	
Standards Compliance	DVB-RC, ITUT J.83 Annexes A, B, and C DAVIC 1.2 part 8, section 7.8; DVS 167, DVS 178
A/D Converter	Internal 10-bit
Symbol Rate	Variable from 0.772 – 7.2 Mbaud
QAM Constellations	16,32,64,128,256 QAM (including DAVIC 256 QAM Map)
QPSK	Differential Decoding
IF Input Frequencies	36 MHz or 44 MHz IF inputs
Output	Multiplexed transport stream output with broadcast channel to Media Access Control units
Additional I/O	Point of Deployment (POD) RX bypass signals
Return Channel	
Standards Compliance	ITU J.112 Annexes A and B; DVB-RC/DAVIC, DOCSIS 1.0 and DOCSIS 1.1, DVS 167, DVS 178
D/A Converter	Internal 10-bit
RF Output	5 MHz to 65 MHz
Modulation	QPSK and 16 QAM
DOCSIS 1.0 Features	Advanced modem pre-equalization of transmit signal Internal CMTS clock synchronization: no VCXO
Additional Features	Programmable RS encoding (T=010; k=16 253) Programmable randomization Programmable unique word/preamble Internal slot timing and burst control Analog and digital gain control
Additional I/O	Point of Deployment (POD) TX bypass signals
Processor and Control	
Internal Microprocessor	117 MHz SPARC V8 processor for Media Access Control software
Clock Generation	Onboard PLL running from a single external crystal
AGC Output	Supports many Variable Gain Amplifier devices, including, but not limited to: Analog Devices AD8321, Lucent Technologies V4911, Anadigics ARA05050 and ARA 1400, Maxim MAX3501
Tuner Control	Implemented via SPI, IDC, or GPIO
Peripherals	
Interface modules	Inter-Device Communications (IDC, Mastermode only), On-chip UART, Serial Peripheral Interface (SPI), PCM/SLIC Interface*, General Purpose I/O (GPIO)
MAC	
Standards Compliance	DOCSIS 1.0/1.1; DVB-RC/DAVIC; DAVIC OOB, DVS 167; DVB Inband; DAVIC Inband, DVS 178
Host	
Slave Mode	PCI, Power PC, Coldfire (5206, 5307), 68K, SH3/4
Master Mode	Coldfire, 68K, Async Flash
Physical	
Input Voltage	3.3V + 5% (tolerates 5V inputs, except SDRAM), 1.8V
Packaging	208-pin PQFP; 308-pin BGA
SPARC Operating Frequency	117 MHz or 88 MHz

* available only in 308 pin BGA package

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